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FORM**

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Total Number of Pages in This Submission

Application Number

10/624,627

Filing Date

July 21, 2003

First Named Inventor

Luan C. Tran

Art Unit

2811

Examiner Name

Jennifer Kennedy

Attorney Docket Number

MI22-2358

**ENCLOSURES (Check all that apply)**

- |  |   |   |
|--|---|---|
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**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

Firm or Individual Jennifer J. Taylor, Ph.D.; Reg. No. 48,711; Wells St. John P.S.

Signature

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EL979950021



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. .... 10/624,627  
Filing Date .... July 21, 2003  
Inventor .... Luan C. Tran  
Assignee .... Micron Technology, Inc.  
Group Art Unit .... 2811  
**priority** Examiner .... Kennedy, Jennifer J.  
Attorney's Docket No. .... MI22-2358  
Title: Methods of Forming Semiconductor Constructions

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

References –See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR § 1.56. Copies of the cited art are included with the exception of U.S. patents and published U.S. applications (1276 OG 55). No admission is made regarding whether all the submitted references are prior art.


This Supplemental Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing date of a first Office Action, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.

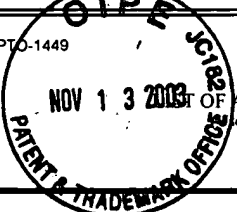
Respectfully submitted,

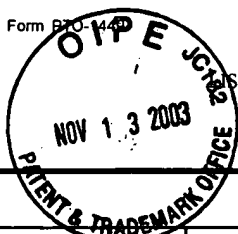
Dated: November 11, 2003

By: Jennifer J. Taylor  
Jennifer J. Taylor, Ph.D.  
Reg. No. 48,711

EL 979950021

Form PTO 1546 		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2358		SERIAL NO. 10/624,627	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran			
FILING DATE July 21, 2003				GROUP 2811			
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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	AB	6,033,952	03-2000	Yasumura, et al.			
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							Yes      No
	AM	EP 0718881	06/96	EPO, Chan			
	AN						
	AO						
	AP						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		Watanabe, H. et al., <i>Novel 0.44μm<sup>2</sup> Ti-Salicide STI Cell Technology for High-Density NOR Flash Memories and High Performance Embedded Application</i> , IEEE 1998, pp. 36.2.1 - 36.2.4.				
	AS		Wolf, S., <i>"Silicon Processing for the VLSI Era"</i> , Vol. 2, pp. 632-635.				
	AT		MITSUBISHI ELECTRIC WEBSITE: Reprinted from website <a href="http://www.mitsubishielectric.com/r_and_d/tech_showcase/ts8.php">http://www.mitsubishielectric.com/r_and_d/tech_showcase/ts8.php</a> on 3/29/2001: "8. Production Line Application of a Fine Hole Pattern-Formation Technology for Semiconductors", on 3/29/2001, 4 pgs				
EXAMINER				DATE CONSIDERED			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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				APPLICANT Luan C. Tran			
				FILING DATE July 21, 2003		GROUP 2811	
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		Document Number	Date	Country	Class	Subclass	Translation
							Yes    No
	AM						
	AN						
	AO						
	AP						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from <a href="http://www.semiconductor.net/semiconductor/issues/1999/sep99/docs/feature1.asp">http://www.semiconductor.net/semiconductor/issues/1999/sep99/docs/feature1.asp</a> on 3/29/2001: "Resists Join the Sub-λ Revolution", 9 pgs.				
	AS		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from <a href="http://www.semiconductor.net/semiconductor/issues/1999/aug99/docs/lithography.asp">http://www.semiconductor.net/semiconductor/issues/1999/aug99/docs/lithography.asp</a> on 3/29/2001: "Paths to Smaller Features", 1 pg.				
	AT		Wolf, S., "Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press 1986, pp. 434-437.				
EXAMINER				DATE CONSIDERED			
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					FILING DATE July 21, 2003		GROUP 2811	
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*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
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	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							
FOREIGN PATENT DOCUMENTS								
	Document Number	Date	Country	Class	Subclass	Translation		
						Yes	No	
	AM							
	AN							
	AO							
	AP							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
	AR		<i>"Session 18: Integrated Circuits and Manufacturing - DRAM and Embedded DRAM Technology," 2001 IEDM Technical Program, 2001 IEEE International Electron Devices Meeting, Dec. 4, 2001, reprinted 11/15/01 from <a href="http://www.his.com/~iedm/techprogram/sessions/s18.html">http://www.his.com/~iedm/techprogram/sessions/s18.html</a>, pp. 1-2.</i>					
	AS							
	AT							
EXAMINER				DATE CONSIDERED				
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